GSXO1202 Ultra-low Jitter Clock
Ultra-low Noise LVDS / PECL in 5 x 7 x 1.8 mm SMD

Features

32 to 200 MHz for LVPECL
106.25 to 200 MHz for LVDS

Phase Jitter (Less than 0.100 ps for LVPECL outputs)

Phase Jitter (Less than 0.130 ps for LVDS outputs)

3.3V supply
Enable / Disable Function (Pad 1 or 2)

Picture of Part

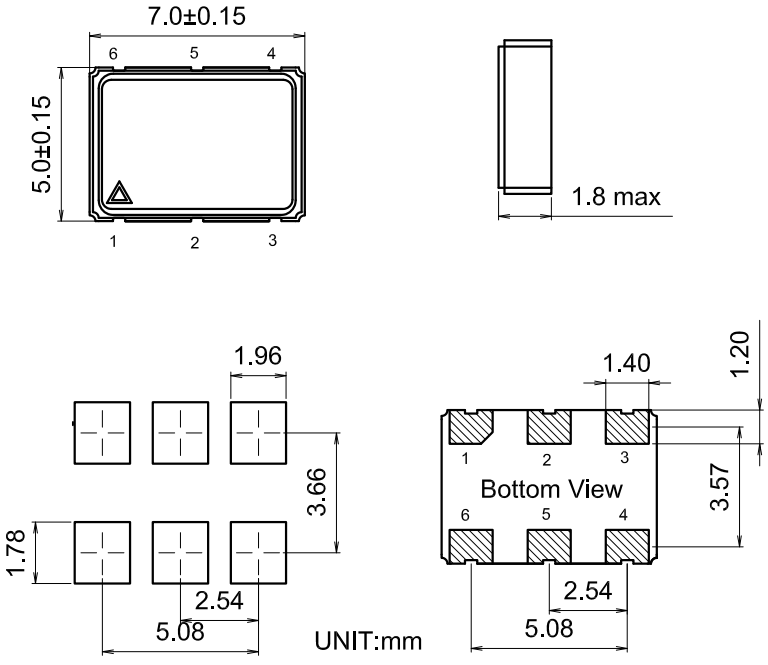
Typical Applications

Telecom Broadband Access
10 Gigabit Ethernet, Fiber Channel
A/D, D/A, FPGA
Storage Area Networking
Test and Measurement

Description

The GSXO1202 family offers ultra-low phase jitter with either PECL or LVDS outputs required to maximize performance in today's next generation digital signal processing and data communications IC chipsets.

Mechanical Drawing and PIN Connections



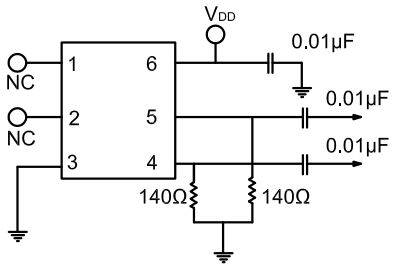
Pin#	Symbol	Function
1	NC	No Internal Connection is made
2	NC	No Internal Connection is made
3	GND	Electrical and Lid Ground
4	f_o	Output Frequency
5	Cf_o	Complementary Output Frequency
6	V_{DD}	Supply Voltage

Specification

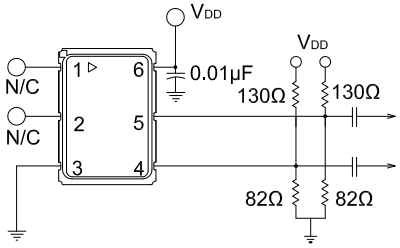
GSXO1202		Sym.	Condition	Value			Unit	Note
				Min.	Typ.	Max.		
Operational Frequency Range				32		200	MHz	For LVPECL
Operational Frequency Range				106.25		200		For LVDS
LVPECL	LOAD		50 ohms into Vcc -1.3V					
		V_H	H - level voltage	Vcc-1.085		Vcc-0.888	V	Levels take into account operating Temperature variation
		V_L	L - level voltage	Vcc-1.830		Vcc-1.555	V	
			Rise & Fall time			1.00	ns	
LVDS			Output Differntial Voltage	247	355	454	mV	
			DC Offset Voltage	1.125	1.250	1.375	V	
			Rise & Fall time			1.0	ns	
LVDS Output Load			100 ohms Differential					
DC Supply Voltage				3.15	3.30	3.45	V	
DC Supply Current			DC Currents under NO LOAD Condition		50 37	65 45	mA	LVPECL LVDS
Frequency stability vs. temperature			-40°C to +85°C, ref 25C	-50		+50	ppm	25 and 100 ppm available
PECL / LVDS @156.25 MHz			100 Hz offset		-110		dBc/Hz	
			1000 Hz		-137			
			10 KHz		-151			
			100 KHz		-159			
			1 MHz		-161			
Phase Jitter (12KHz to 20 MHz)			**@156.25MHz**		0.065	0.130	ps	
Enable	Pin 2		Pin 2 as NO CONNECT	2.8			V	RF Outputs Enabled
Disable			Is Enable by default			0.4	V	RF Outputs disabled

Environmental, mechanical conditions.	
Operating temperature range	**-40℃ to +85℃ maximum range available**
Storage temperature range	**-50℃ to 125℃**
TEMPERATURE CYCLE	MIL-STD 883 METHOD 1010
Mechanical shock	MIL-STD 883 METHOD 2002
Vibration	MIL-STD 883 METHOD 2007
Soldering	MIL-STD 883 METHOD 2003

LVPECL Application Diagrams

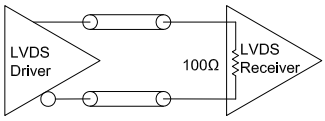


Single Resistor Termination Scheme

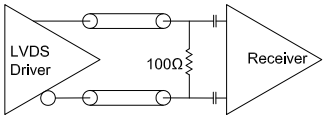


Pull-Up Pull Down Termination

LVDS Application Diagrams



LVDS to LVDS Connection, Internal 100ohm Resistor



LVDS to LVDS Connection

Ordering Information

GSXO1202-XXX.XXXXXX-W-Y-Z

1. Field " XXX.XXXXXX " is the Output Frequency to six decimals in MHz
2. Field " W " is Operating Temperature Range and Freq. Stability :
   a. " 0 " for -40°C to +85°C and +/- 25 ppm
   b. " 1 " for -40°C to +85°C and +/- 50 ppm
   c. " 2 " for -40°C to +85°C and +/- 100 ppm

   ***NOTE: Inclusive of 25C tolerance, drift over temperature, aging, Variation with load and voltage, shock, vibration, and reflow.

3. Field " Y " is for option for PECL or LVDS :
   a. " 0 " for PECL Outputs
   b. " 1 " for LVDS Outputs
4. Field " Z " is for option to have Enable / Disable Function
   a. " 0 " for E/D Function on Pad 1 or Pad 2
   b. " 1 " for Pad 1 and Pad 2 are NC (no connection internally)

Part Number Example

GSXO1202-622.080000-1-1-1
622.080000 MHz Operating Frequency
Operating Temperature of -40°C to +85°C
+/- 50 ppm Frequency Stability
LVDS Outputs
No Enable / Disable (Pad 1 and Pad 2 are NC)