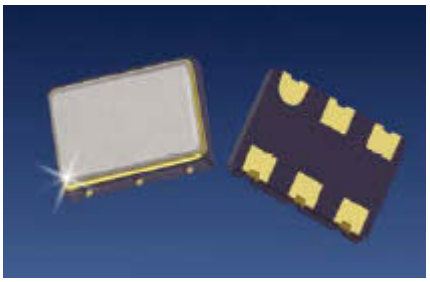
GSVX1206 LVDS / PECL
Voltage-controlled SAW oscillator 5 x 7.5 x 2.0 mm

Features

212.5 to 800 MHz
Phase Jitter (0.100 ps typical)
Across 12KHz to 20 MHz bandwidth
LV-PECL or LVDS complimentary outputs
3.3V operation
Output Disable Function
Improved Temperature Stability over Standard VCSO

Picture of Part



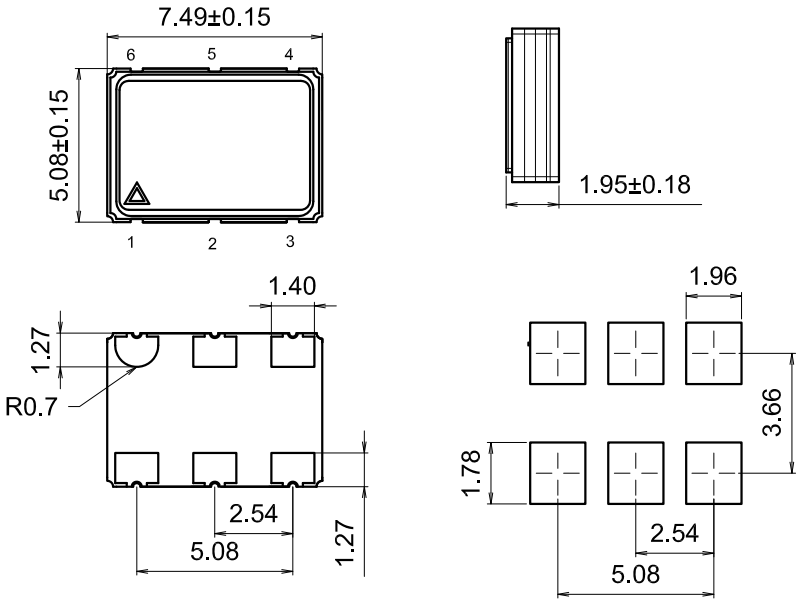
Typical Applications

10 Gigabit Fiber Channel
10 Gigabit Ethernet LAN / WAN
Test and Measurement
OC-192 ; SONET / SDH

Description

The GSVX1206 family offers ultra-low phase jitter with either LV-PECL or LVDS outputs required to maximize performance in today's next generation PLL circuits used for clock smoothing and frequency translation.

Mechanical Drawing and PIN Connections



Pin	Symbol	Function
1	V_C	VCXO
2	OE[1]	Enable = High (or Vcc), Disable = Output Low
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{cc}	Power Supply Voltage (3.3V ±10%)

Note 1: For proper operation disable pin can not be left floating.

Specification

GSVX1206		Sym.	Condition	Value			Unit	Note
				Min.	Typ.	Max.		
Operational Frequency Range				212.5		800	MHz	
LVPECL		Iout	Additional DC current with both Outputs under load			20	mA	
		Vmid	Mid - level voltage	Vcc-1.40	Vcc-1.25	Vcc-1.00	V	Levels take into account operating Temperature variation
		Pk-pk	Peak to peak swing	450	600	750	mV	
LVDS		Vmid	Mid - level voltage	Vcc-2.50	Vcc-2.40	Vcc-2.30	V	
		Pk-pk	Peak to peak swing	250	350	450	mV	
			Rise & Fall time		250	500	ps	Measured from 20% to 80%
			Symmetry		50 +/- 5 %			Of full output swing
DC Supply Voltage DC Supply Current			DC Current under NO LOAD Condition	2.97	3.30 55	3.63 70	V mA	
Control Voltage Function			Absolute Pull Range (APR) Gain transfer (Kv)	+/- 50	 +100		PPM ppm/v	
			Control Voltage Range	0.3		3.0	V	
			Input Impedance Modulation BW	75 50			Kohm KHz	
Frequency Stability					+/- 20		PPM	
PECL / LVDS @622.08 MHz			1000 Hz		-110		dBc/Hz	
			10 KHz		-130			
			100 KHz		-134			
			1 MHz		-138			
			20 MHz		-147			
Phase Jitter (12KHz to 20 MHz)			**@622.08MHz**		0.100	0.250	ps	
Enable Disable	Pin 2			2.8		 0.4	V V	RF Outputs Enabled RF Outputs disabled
Environmental, mechanical conditions.								
Operating temperature range			**-40℃ to +85℃ maximum range available**					
Storage temperature range			**-55℃ to 125℃**					
Mechanical shock			MIL-STD 883 METHOD 2002					
Vibration			MIL-STD 883 METHOD 2007					
Soldering			MIL-STD 883 METHOD 2003					

Ordering Information

GSVX1206-XXX.XXXXXX-W-Y

1. Field " XXX.XXXXXX " is the Output Frequency to six decimals in MHz

2. Field " W " is for minimum APR :
   a. " 0 " for +/- 50 ppm
   b. " 1 " for +/- 80 ppm
   c. " 2 " for +/- 100 ppm

   ***NOTE: APR is pull range above and beyond 25C tolerance, drift over temperature, aging, variation with load and voltage, shock, vibration, and reflow.

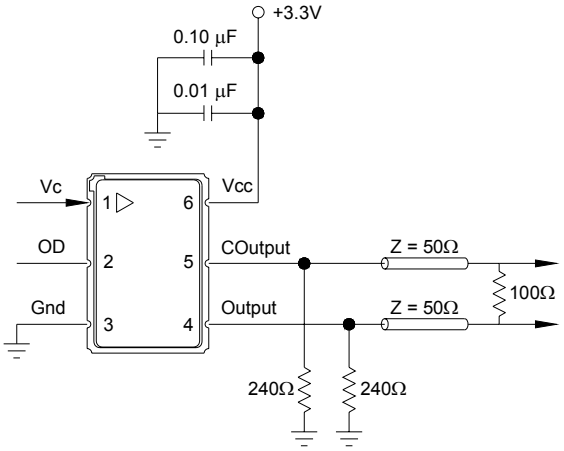
3. Field " Y " is Option between LV-PECL or LVDS :
   a. " 0 " for LV-PECL Outputs
   b. " 1 " for LVDS Outputs

Standard Output Frequencies (MHz)

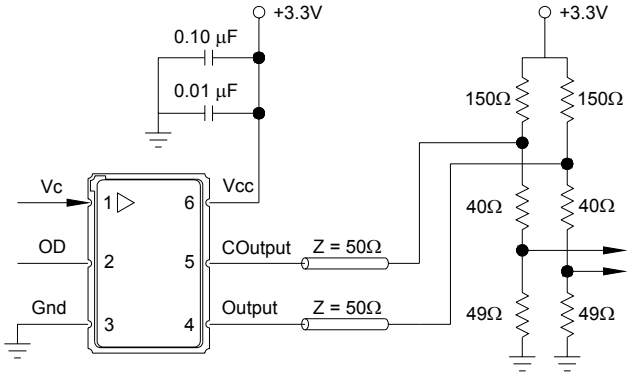
*155.5200	*156.2500	*160.0000	*175.0000	*187.5000	*194.8000	*200.0000	212.5000
240.0000	245.7600	250.0000	311.0400	312.5000	320.0000	324.0000	350.0000
375.0000	389.6000	400.0000	425.0000	480.0000	491.5200	500.0000	531.2500
537.6000	600.0000	622.0800	625.0000	644.5313	657.4219	666.5143	669.3266
672.1627	690.5692	693.4830	704.3806	707.3527	720.0000	768.0000	796.8750

Frequencies not shown are available upon request.

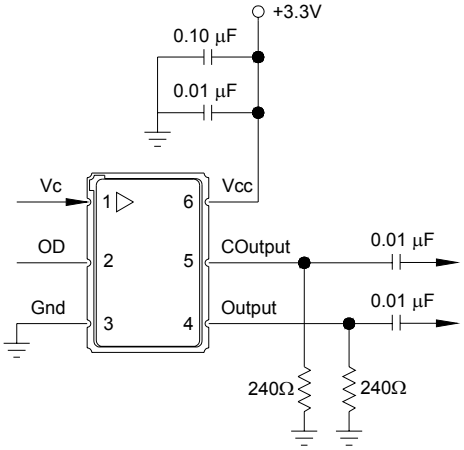
Suggested Output Load Configurations



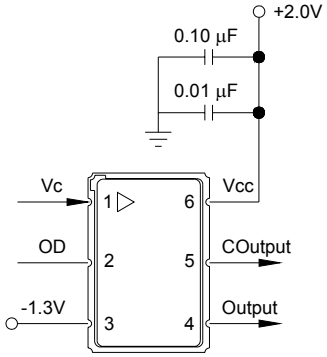
LV-PECL to LV-PECL: For short transmission lengths, the power consump ion could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.



Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplys as shown.